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NAVAL TACTICAL DATA SYSTEM

FUNCTIONAL SPECIFICATION

CHANGE ORDER

NO. ONE

for

TECHNICAL NOTE NO. 244

AN/USQ-20

UNIT COMPUTER CHARACTERISTICS

PX 1343-38

Remington Rand Univac®

DIVISION OF SPERRY RAND CORPORATION

UNIVAC PARK, ST. PAUL 16, MINNESOTA

NAVY DEPARTMENT

BUREAU OF SHIPS

ELECTRONICS DIVISIONS

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INSTRUCTIONS: *Staple Change Order to Document or Enter Revisions in Text.*

Approved: L. D. Findley
 L. D. Findley
 Manager
 Naval Tactical Data System

PAGE	LOCATION	CORRECTION																																																														
5	In Figure 2 Upper right-hand section	R' should be R*																																																														
A-3	Line 5	Remove "D" after "14"																																																														
A-4	Top of Table A-1	Add "(OCTAL)" after "CODE" in both instances																																																														
A-5	Upper right-hand cor- ner of Table A-2	<table border="1"> <thead> <tr> <th rowspan="2">f</th> <th colspan="3">j=0,1 NORMAL</th> <th colspan="3">j=0 REPEAT</th> </tr> <tr> <th>k=0,4</th> <th>k=7</th> <th>k≠0,4,7</th> <th>k=0,4</th> <th>k=7</th> <th>k≠0,4,7</th> </tr> </thead> <tbody> <tr> <td>01</td> <td>9.6/12.8</td> <td>11.2/14.4</td> <td>16</td> <td></td> <td></td> <td></td> </tr> <tr> <td>02</td> <td>9.6/12.8</td> <td>11.2/14.4</td> <td>16</td> <td></td> <td></td> <td></td> </tr> <tr> <td>03</td> <td>11.2/16</td> <td>11.2/16</td> <td>16/20.8</td> <td></td> <td></td> <td></td> </tr> <tr> <td>04</td> <td>12.8</td> <td>11.2</td> <td>16</td> <td>9.6</td> <td>8.0</td> <td>11.2</td> </tr> <tr> <td>05</td> <td>9.6/12.8</td> <td>9.6/12.8</td> <td>16</td> <td></td> <td></td> <td>R</td> </tr> <tr> <td>06</td> <td>9.6/12.8</td> <td>9.6/12.8</td> <td>16</td> <td></td> <td></td> <td>R</td> </tr> <tr> <td>07</td> <td>11.2/16</td> <td>11.2/16</td> <td>16/20.8</td> <td></td> <td></td> <td>R</td> </tr> </tbody> </table>	f	j=0,1 NORMAL			j=0 REPEAT			k=0,4	k=7	k≠0,4,7	k=0,4	k=7	k≠0,4,7	01	9.6/12.8	11.2/14.4	16				02	9.6/12.8	11.2/14.4	16				03	11.2/16	11.2/16	16/20.8				04	12.8	11.2	16	9.6	8.0	11.2	05	9.6/12.8	9.6/12.8	16			R	06	9.6/12.8	9.6/12.8	16			R	07	11.2/16	11.2/16	16/20.8			R
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A-6	Under "B. FUNCTION CODE DESIGNATOR -f" lines 4 and 5	Replace "00014" with "00000" in line 4 Replace "00014" with "00000" in line 5																																																														

FUNCTIONAL SPECIFICATION CHANGE ORDER (Cont.)

PAGE	LOCATION	CORRECTION
A-9	Under "H. <i>MAGNETIC CORE MEMORY ASSIGNMENT</i> ", last line	Replace "three" with "two", and "eight" with "seven"
A-10	Line 1 Lines 2 through 8 First line under "I. <i>WIRED MEMORY</i> " Line 4 from bottom of page Line 2 from bottom of page	Delete the whole line Change "2)" to "1)", "3)" to "2)", "4)" to "3)", "5)" to "4)", "6)" to "5)", "7)" to "6)", and "8)" to "7)" at the beginnings of lines 2 through 8. Remove "D" after "16" Replace "00014" with "00000" Replace "14" with "00"
A-12	Footnote	Remove "D" after "59"
A-13	Footnote	Remove "D" after "59"
A-14	"17 <i>STORE Cⁿ</i> " Footnote	Place asterisk (*) after " <i>Cⁿ</i> " Add the following as a footnote: *"Instruction 17, <i>STORE Cⁿ</i> is intended for use in the computer's reply to an interrupt; consequently, it is not synchronized with the input buffering process. Therefore, the execution of <i>n</i> sequential Instruction 17's on the same channel, will not place <i>n</i> sequential <i>Input Acknowledge</i> signals on the <i>Input Acknowledge</i> line associated with that channel. It will, in fact, generate a signal which is <i>n</i> x 14.8 microseconds wide on that <i>Input Acknowledge</i> line. Moreover, it is obvious that the execution of an Instruction 17 on a given channel while an <i>Input</i> buffer is in progress on the channel will, in most cases, seriously interfere with the buffered transfer of data. It should be noted, how-

FUNCTIONAL SPECIFICATION CHANGE ORDER (Cont.)

PAGE	LOCATION	CORRECTION
A-14	Footnote	<p>ever, that any other instruction executed between two Instruction 17's will allow the <i>Input Acknowledge</i> line to return to the logical <i>zero</i> state for a time consistent with Input/Output specifications before it rises a second time."</p>
A-18	Under "53 <i>SELECTIVE SUBSTITUTE</i> "	<p>Add the following after the last line:</p> <p>"In this instruction repeated, K = 0 or K = 4 should not be used."</p>
A-21	<p style="text-align: center;">Line 1</p> <p style="text-align: center;">Under "<i>RETURN JUMP (Manual)</i>", line 7</p> <p style="text-align: center;">Footnote</p>	<p>Place asterisk (*) at end of line after "Y + 1"</p> <p>Place asterisk (*) at end of line 7 after "Y + 1"</p> <p>Add the following as a footnote:</p> <p>"*This instruction is the normal sequence of events; that is, this sequence occurs when the Return Jump instruction is executed in the context of a program which is proceeding from one instruction to the next by way of skips, jumps, or any programmed branching.</p> <p>However, if the Return Jump immediately follows recognition, by the Control Section of the computer, of an interrupt (that is, if the Return Jump is the instruction stored at the Interrupt Entrance Register), then it must be described as follows:</p> <p style="padding-left: 40px;">"Store (P)_p in the lower half of memory address \bar{Y}. Then jump to Y + 1."</p> <p>The p-designator controls the modification of (P) and it is set up by the instruction immediately preceding the Return Jump caused by the interrupt. Therefore, the Return Jump causes the storage of the address of the next sequential instruction which would have been executed if the interrupt had not occurred.</p>

FUNCTIONAL SPECIFICATION CHANGE ORDER (Cont.)

PAGE	LOCATION	CORRECTION
A-21	Footnote	In fact, the general description of the Return Jump is the latter, with the understanding that, in the non-interrupt case, p is set to <i>one</i> , which causes the storing of P + 1 in Y."
B-3	Paragraph that immediately follows item "2) g)"	<p>Replace the paragraph with the following:</p> <p>"Note that the <i>Input Acknowledge</i> is the computer response to either an <i>Input Data Request</i> or to an <i>Interrupt</i>. To eliminate misinterpretation of the <i>Input Acknowledge</i> signal, peripheral equipment must not interrupt until its last <i>Input Data Request</i> has been acknowledged by the computer. Under emergency conditions, when data loss is of secondary importance, the <i>Input Data Request</i> may be dropped and the Interrupt raised a minimum of 100 microseconds later. When these conditions prevail, an <i>Input Acknowledge</i> signal that occurs after the Interrupt is raised will be an answer to the Interrupt."</p>
B-4	Line 1 Line 2	<p>Line is corrected to read,</p> <p style="padding-left: 40px;">"c) Computer detects Output Data Request."</p> <p>Line is corrected to read,</p> <p style="padding-left: 40px;">"d) Computer (at its convenience) places information on the 30 data lines."</p>
B-6	Line 3	<p>After "lines" and before "The", insert:</p> <p style="padding-left: 40px;">"To ensure that data will be accepted."</p> <p>Also change "The" to "the".</p>

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